

Switch Receiver Transceiver

Controller Sc
6

FIG. 2

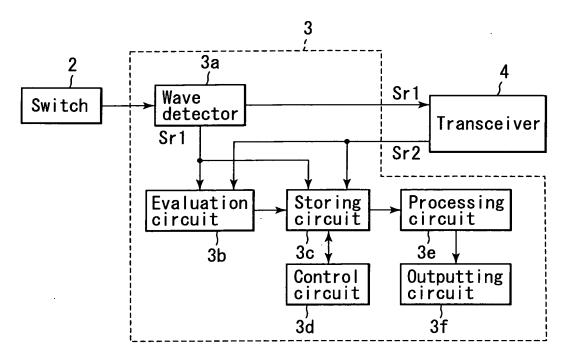


FIG. 3

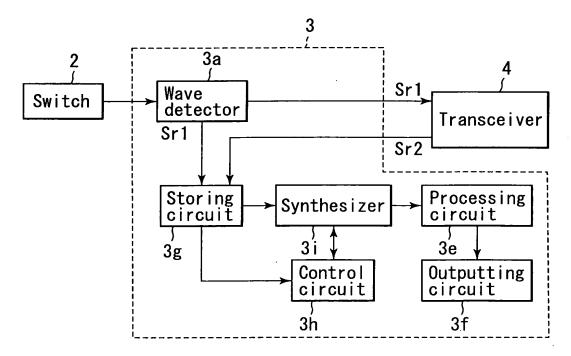
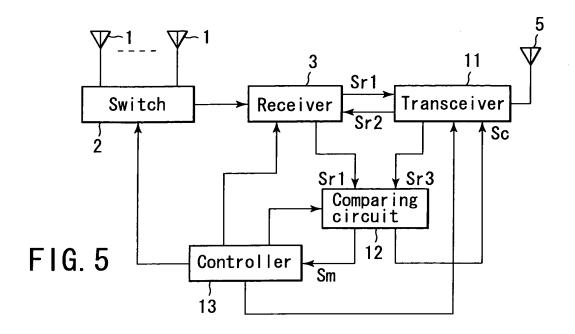


FIG. 4



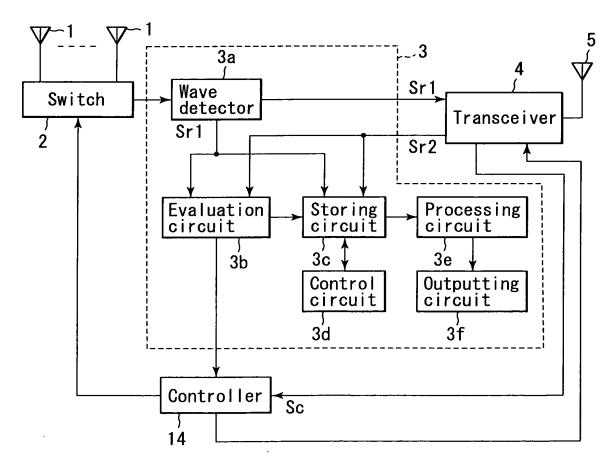


FIG. 9

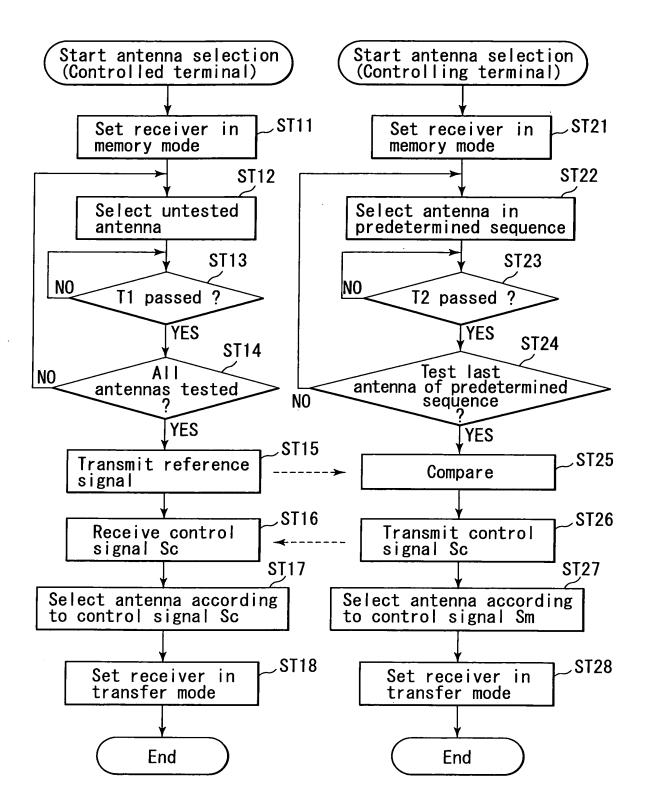


FIG. 6

OBLON, SPIVAK, ET AL DOCKET #: 247242US2SRD INV: Shuichi SEKINE, et al. SHEET <u>5</u> OF <u>6</u>

| | #1a | #1b | #2a | #2b | #3a | #3b | #4a | #4b |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| #1a | _ | 0 | Δ | 0 | 0 | 0 | 0 | 0 |
| #1b | _ | - | 0 | Δ | 0 | 0 | 0 | 0 |
| #2a | _ | 1 | - | Δ | Δ | Δ | Δ | Δ |
| #2b | _ | _ | | 1 | Δ | Δ | Δ | Δ |
| #3a | - | 1 | - | - | - | 0 | Δ | 0 |
| #3b | _ | _ | _ | _ | - | 1 | 0 | Δ |
| #4a | _ | _ | - | - | _ | _ | _ | Δ |
| #4b | _ | _ | _ | _ | _ | - | _ | - |

O:Terminal #1 is in charge

△:Terminal #2 is in charge

FIG. 7

| | #1a | #1b | #2a | #2b | #3a | #3b | #4a | #4b |
|-----|-----|----------|-----|-----|-----|-----|-----|-----|
| #1a | _ | 0 | Δ | 0 | × | 0 | | 0 |
| #1b | _ | - | 0 | Δ | 0 | × | 0 | |
| #2a | _ | <u> </u> | _ | Δ | × | Δ | | Δ |
| #2b | _ | - | 1 | 1 | Δ | × | Δ | |
| #3a | - | _ | - | _ | 1 | × | | × |
| #3b | - | - | - | - | _ | - | × | |
| #4a | _ | _ | _ | _ | _ | - | _ | |
| #4b | | - | - | _ | | _ | _ |] |

O:Terminal #1 is in charge

- △:Terminal #2 is in charge
- ×:Terminal #3 is in charge
- □:Terminal #4 is in charge

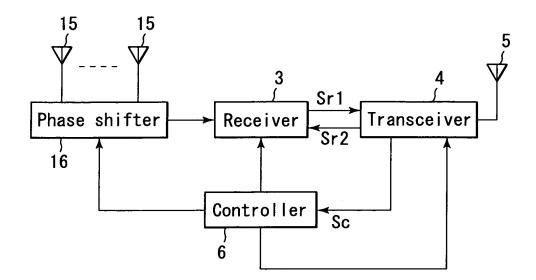


FIG. 10

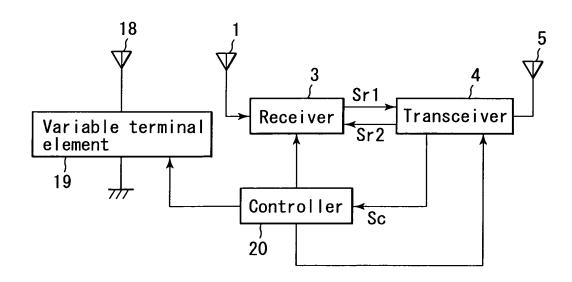


FIG. 11